700MHz-2700MHz, 30W, 28V RF Power LDMOS FETs

Description

The ITCH24025E2 is a 30-watt, internally matched LDMOS FET, designed for cellular base station and ISM applications with frequencies from 700MHz to 2700 MHz

ITCH24025E2

- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 200 mA , Pulse Width =10us, Duty Cycle =12%.

Frequency (MHz)	Gp (dB)	P_1dB (dBm)	η D (%)	P_3dB (dBm)	η D (%)
850~900	22	45	64	46	67
1330~1350	18	47	61	47.6	65
1805~1880	19	46	59	47	61
2400~2500	20	44	55	45	57
2620~2690	18.5	45	53	46	57

- Typical Performance (On Innogration fixture with device soldered): VDD = 32 Volts, IDQ = 350 mA, Test signal: WCDMA, 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz,PAR =10.5 dB at 0.01 % probability on CCDF.

Frequency (MHz)	$P_{L(AV)}$ (W)	Gp (dB)	η D (%)	$ACPR_{5M}$ (dBc)	$ACPR_{10M}$ (dBc)
2110	3	17.3	16	-46.7	-57.7
2140	3	17.6	16	-46.5	-57.6
2170	3	18	16	-46.4	-57.6

Highlight: The fixture is used same board different BOM.

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	1.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=0V; I_{DS}=1mA	V_{DSS}	65			V
Zero Gate Voltage Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}			1	μA
Gate--Source Leakage Current	V_{GS} = 9 V, V_{DS} = 0 V	I_{GSS}			1	μA
Gate Threshold Voltage	V_{DS} = 28V, I_D = 300 μA	$V_{GS}(th)$		1.75		V
Gate Quiescent Voltage	V_{DS} = 28 V, I_{DS} = 200 mA, Measured in Functional Test	$V_{GS(Q)}$		2.7		V

Pulse CW Signal performance (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 200 mA, f = 875 MHz, CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	Gp		20		dB
Drain Efficiency@P3dB	η_D		67		%
3dB Compression Point	P_{-3dB}		46		dBm
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 200 mA, f = 875 MHz

VSWR 10:1 at 30W Pulsed CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

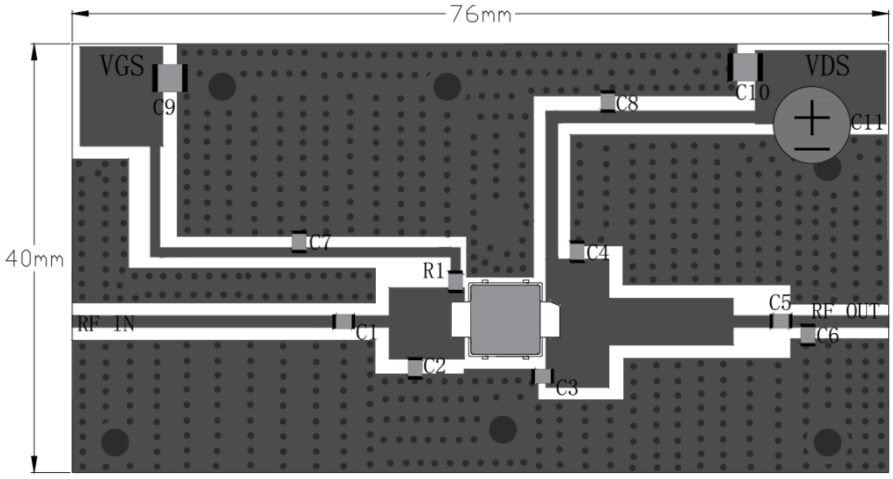


Figure 1. Test Circuit Component Layout(2110~2170MHz)

Table 5. Test Circuit (2010~2170MHz) Component Designations and Values

Component	Description	Suggested Manufacturer	P/N
C1,C5,C7,C8	Ceramic Capacitor,18pF	ATC	600S 180
C2	Ceramic Capacitor,2.2pF	ATC	600S 2R2
C3,C4	Ceramic Capacitor,1.5pF	ATC	600S 1R5
C6	Ceramic Capacitor,0.4pF	ATC	600S 0R4

C9,C10	Capacitor,10uF	Murata	GRM32DF51H106
C11	Electrolytic Capacitor ,470uF,63V	Vishay	MAL203858471E3
R1	Chip Resistor,10Ω	Digi-Key	P10ECT-ND
PCB	0.76mm [0.030''] thick, εr=3.48, Rogers RO4350, 1 oz. copper		

TYPICAL CHARACTERISTICS

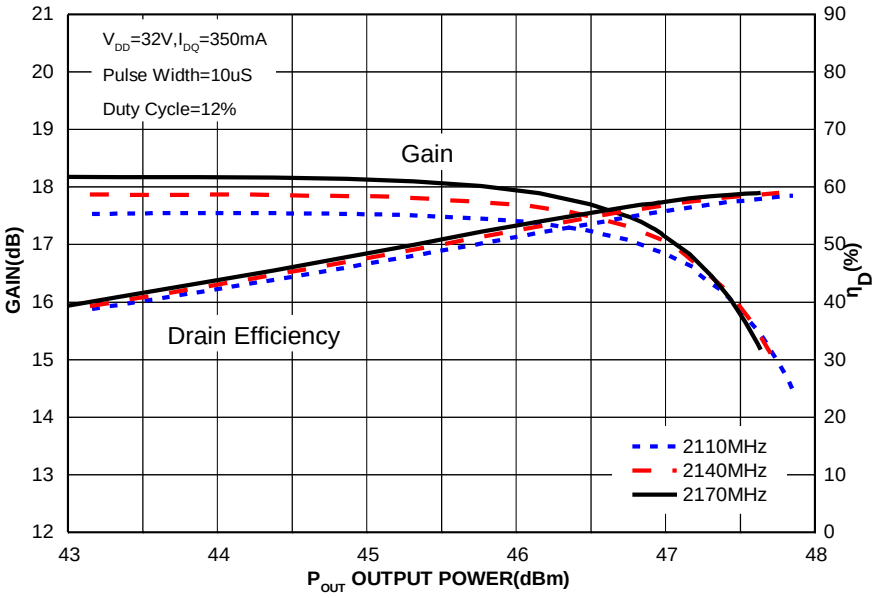


Figure 1. Power gain and drain efficiency as function of Pulse output power（2110-2170MHz）

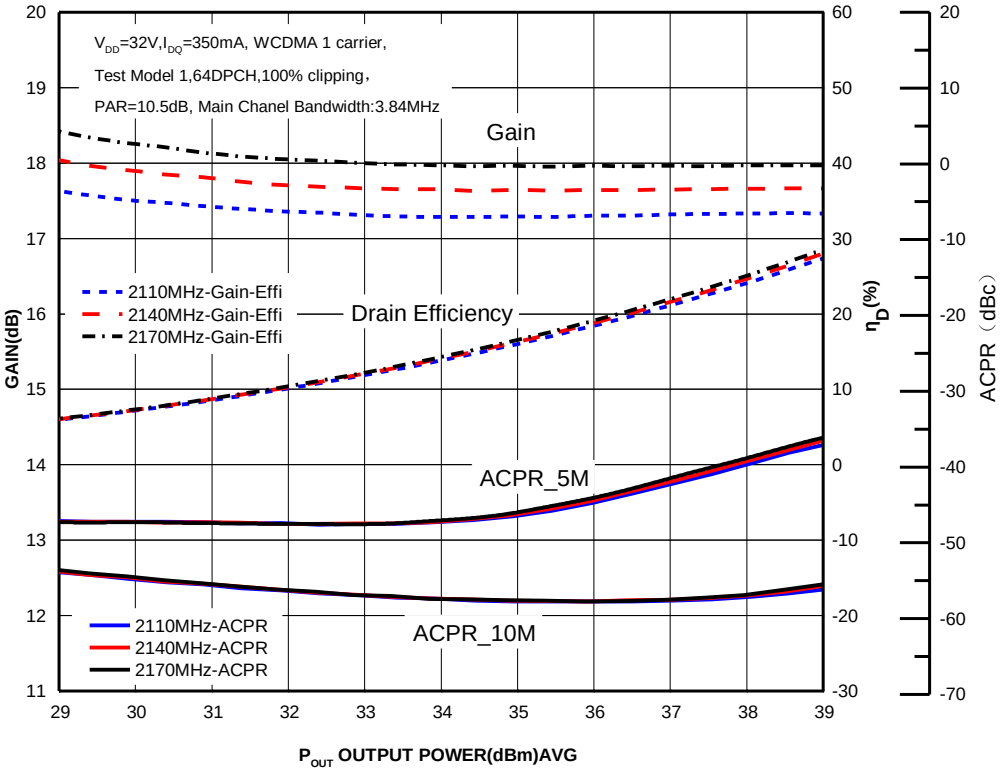


Figure 2. Single−Carrier WCDMA Power gain and drain efficiency and ACPR at 5 MHz and at 10 MHz as function of average output power（2110-2170MHz）

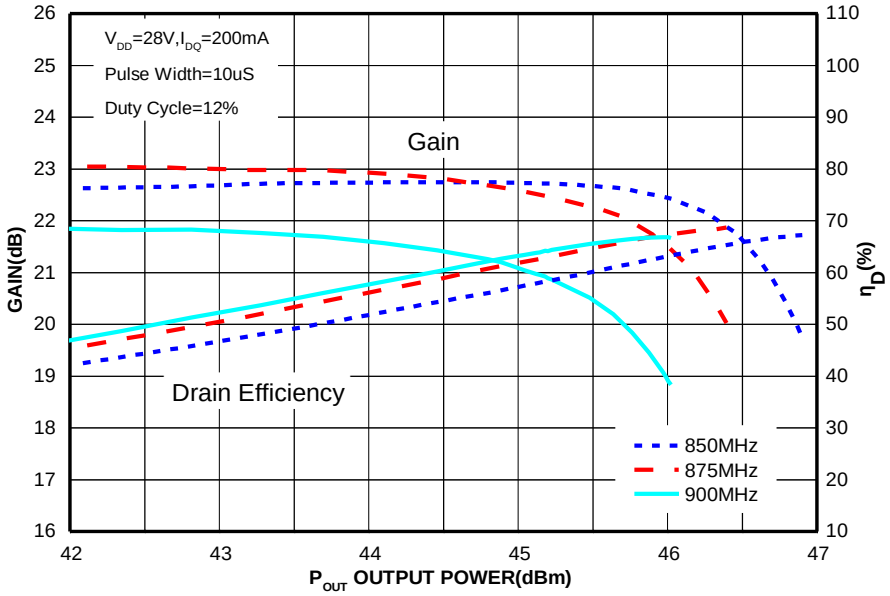


Figure 3. Power gain and drain efficiency as function of Pulse output power（850-900MHz）

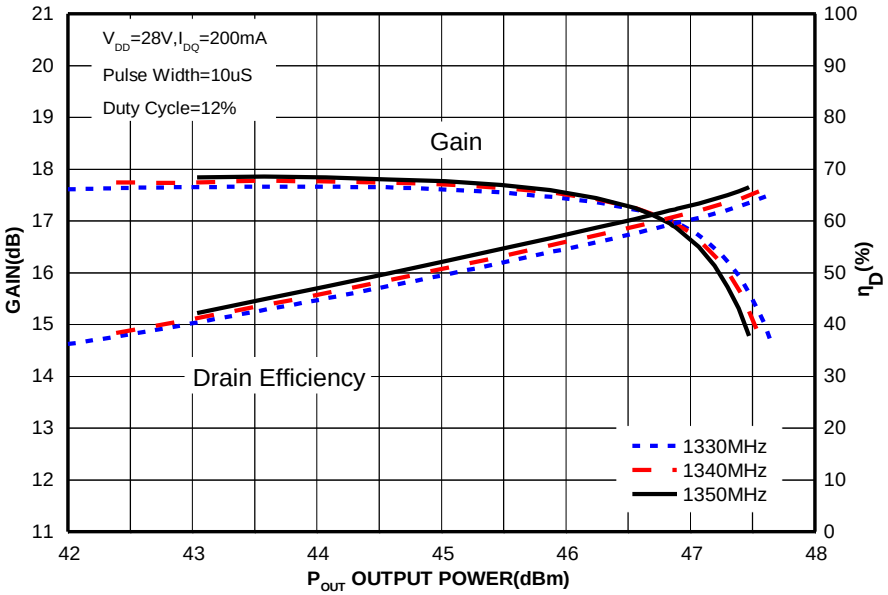


Figure 4. Power gain and drain efficiency as function of Pulse output power（1330-1350MHz）

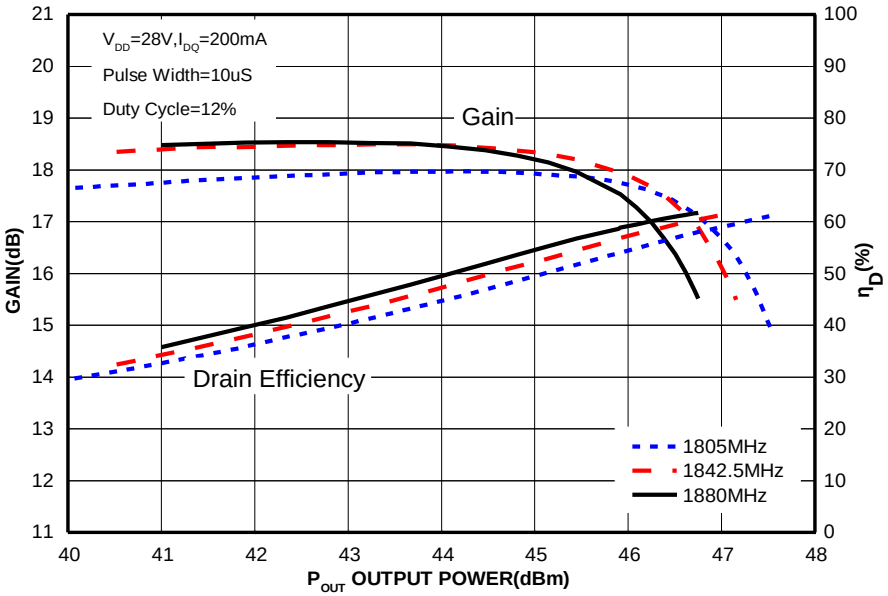


Figure 5. Power gain and drain efficiency as function of Pulse output power（1805-1880MHz）

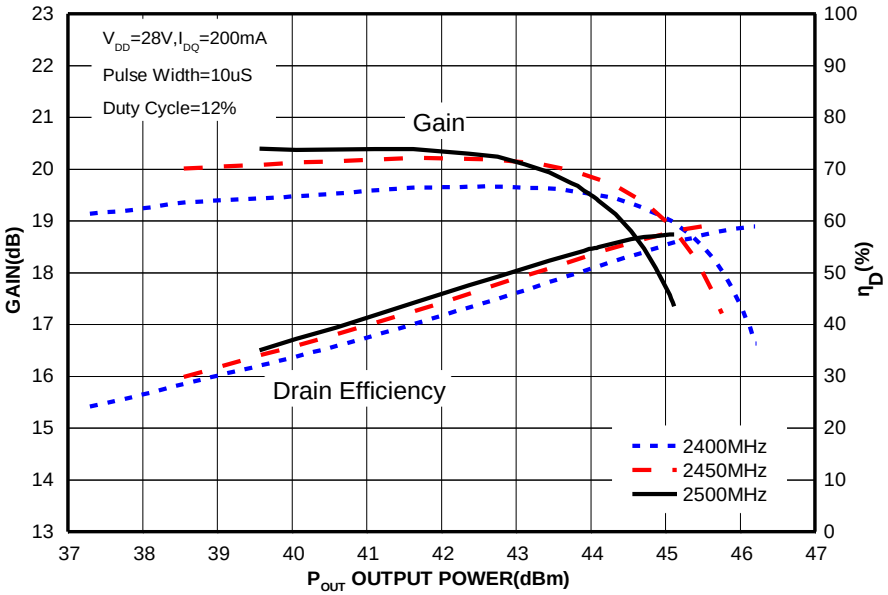


Figure 6. Power gain and drain efficiency as function of Pulse output power（2400-2500MHz）

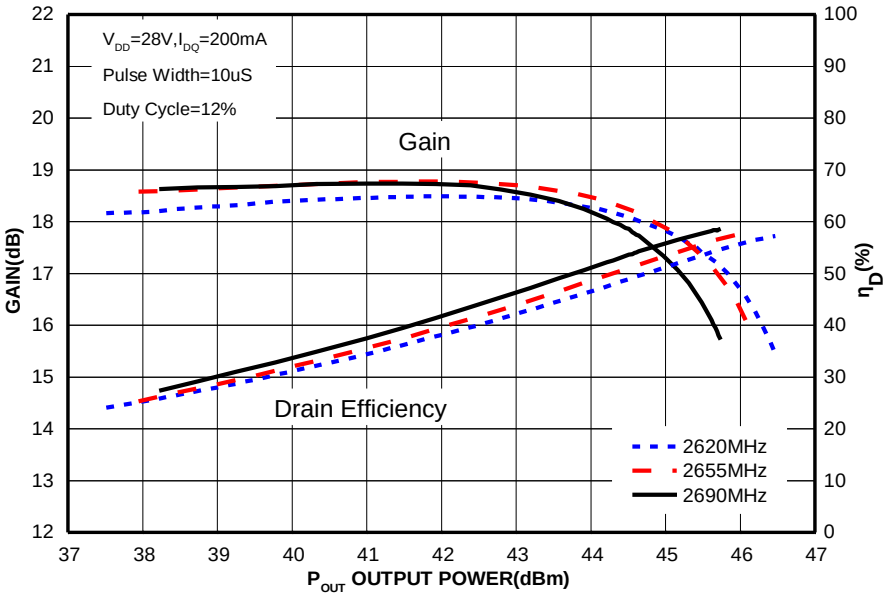
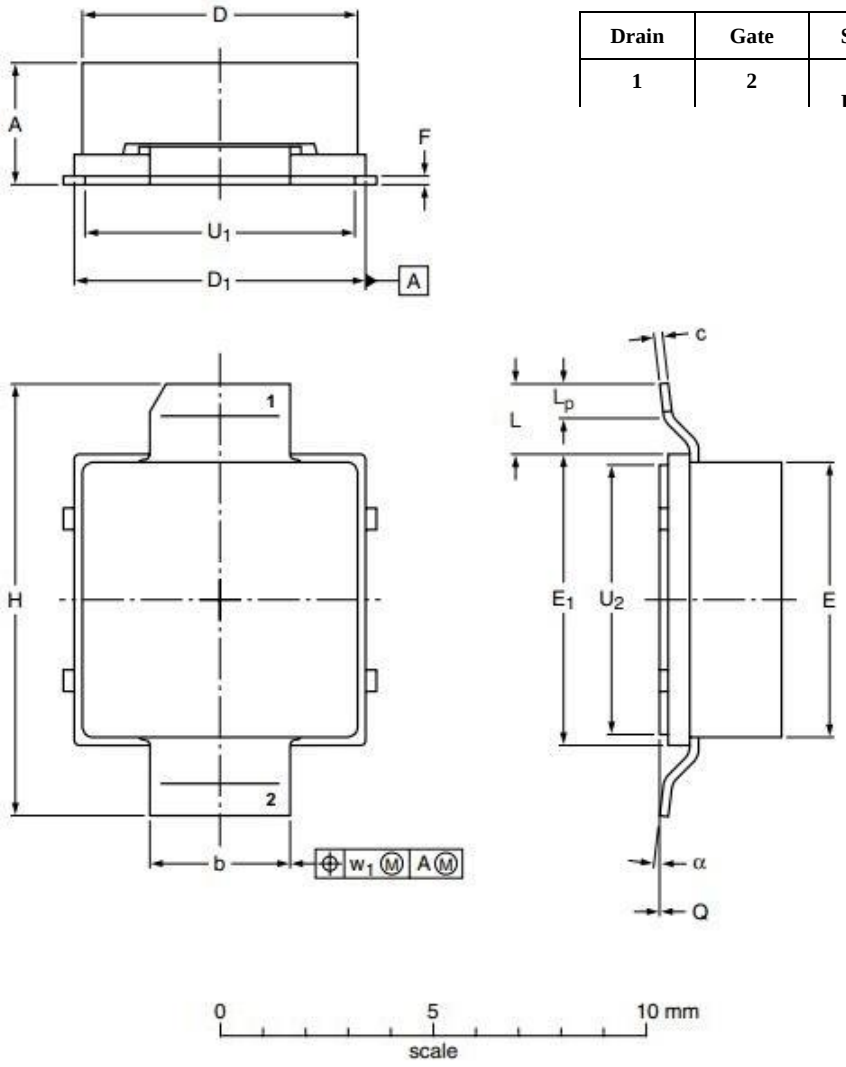


Figure 7. Power gain and drain efficiency as function of Pulse output power（2620-2690MHz）

Package Outline

Earless Flanged ceramic package; 2 leads

Drain	Gate	Source
1	2	Flange



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	L_P	Q	U_1	U_2	w_1	α
mm	3.63 3.05	3.38 3.23	0.23 0.18	6.55 6.40	6.93 6.78	6.55 6.40	6.93 6.78	0.23 0.18	10.29 10.03	1.65	1.02 0.51	+0.05 −0.05	6.43 6.27	6.43 6.27	0.51	7° 0°
inches	0.143 0.120	0.133 0.127	0.009 0.007	0.258 0.252	0.273 0.267	0.258 0.252	0.273 0.267	0.009 0.007	0.405 0.395	0.065	0.040 0.020	+0.002 −0.002	0.253 0.247	0.253 0.247	0.02	7° 0°

OUTLINE VERSION	REFERENCE				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PKG-E-A						10/22/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2016/12/28	**Rev 1.0**	**Preliminary Datasheet**
2017/01/04	**Rev 1.1**	**Preliminary Datasheet**
		Add 2.6G test data.
2017/01/09	**Rev 1.2**	**Preliminary Datasheet**
		Delete ACPR data and graph.
2017/01/19	**Rev 1.3**	**Preliminary Datasheet**
		Add 2.1G test data..
2017/02/06	**Rev 1.4**	**Preliminary Datasheet**
		Add 1.3G test data and test circuit of 2.1G fixture.
2017/02/10	**Rev 2.0**	**Preliminary Datasheet**
		Add 2.1G ACPR data

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